X- and *Ku*-Band Amplifiers Based on Si/SiGe HBT's and Micromachined Lumped Components

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***Abstract*— A double mesa-structure Si/SiGe heterojunction bipolar transistor (HBT) and novel micromachined lumped passive components have been developed and successfully applied to the fabrication of X- and Ku-band monolithic amplifiers. The fabricated 5×5 μm^2 emitter-size Si/SiGe HBT exhibited a dc-current gain β of 109, and f_T and $f_{\max}$ of 28 and 52 GHz, respectively. Micromachined spiral inductors demonstrated resonance frequency of 20 GHz up to 4 nH, which is higher than that of conventional spiral inductors by a factor of two. Single-, dual-, and three-stage X-band amplifiers have been designed, based on the extracted active- and passive-device model parameters. A single-stage amplifier exhibited a peak gain of 4.0 dB at 10.0 GHz, while dual- and three-stage versions showed peak gains of 5.7 dB at 10.0 GHz and 12.6 dB at 11.1 GHz, respectively. A Ku-band single-stage amplifier has also been designed and fabricated, showing a peak gain of 1.4 dB at 16.6 GHz. Matching circuits for all these amplifiers were implemented by lumped components, leading to a much smaller chip size compared to those employing distributed components as matching elements.**

***Index Terms*—Amplifier, HBT, micromachining, MMIC, resonance frequency, SiGe.**

I. Introduction

As THE major application field of microwave circuits shifts from military to commercial markets, monolithic microwave integrated circuits (MMIC's) based on Si technology have received great attention due to their lower cost compared to III–V components. Also attractive as the main advantages of Si MMIC's are the matured Si technology, compatibility with Si CMOS technology, mechanical stability of Si substrate, and superior thermal conductivity of Si. In particular, compatibility with CMOS technology provides the opportunity for the integration of RF modules with low-frequency circuitry. In view of these facts, a proliferation of the Si MMIC market is anticipated in the near future.

The first attempt to fabricate Si-based microwave circuits can be traced back to the 1960's [1]. Since then, however, the development of Si monolithic microwave circuits has been impeded by several obstacles, the most significant of which are the absence of semi-insulating substrate and the inferior operation frequency of Si-based devices. Recently, these two shortcomings have been removed by the availability of the high-resistivity Si substrate and the emergence of high-quality SiGe epitaxial layers. It has been reported that the dominant factor in transmission-line loss is conductor loss, rather than dielectric loss, if the resistivity of the substrate is close to or higher than 10 k$\Omega \cdot$ cm [2]. Fortunately, matured impurity control techniques at the present time have led to the production of Si substrate with $\rho > 10$ k$\Omega \cdot$ cm, so that the lossy substrate may not be a limitation for Si MMIC's. On the other hand, recent advances in the growth of epitaxial SiGe layers have led to high-quality Si/SiGe heterojunctions and, consequently, to high-performance Si-based devices employing these heterojunctions. This development of Si/SiGe device technology, especially that of Si/SiGe HBT's, has pushed the operating frequency of these devices to higher than 100 GHz, approaching that of GaAs-based devices and eliminating the remaining limitation for Si MMIC's [3]–[5].

Owing to the breakthrough in Si-based device technology, there have been a number of reports on successful implementation of Si/SiGe HBT-based MMIC's operating at X-band or at even higher bands. Voltage-controlled oscillators (VCO's) with oscillation frequency of 26 and 40 GHz [6] and X-band mixers [7] have been realized based on Si/SiGe HBT's. A narrow-band amplifier at Ka-band [8] and a wide-band amplifier up to Ku-band [9] have also been implemented with Si/SiGe HBT's. However, all these circuits are designed with distributed matching components, resulting in rather large circuit areas. For large-scale integration of circuits, which is essential in future commercial applications, reduction of chip size is critical. This can be achieved by employing lumped components as matching elements, owing to their smaller dimensions compared with distributed ones up to 30 GHz. Lumped components, however, generally suffer from low-resonance frequency and this limits the frequency range of lumped matching circuits. This strongly motivates the development of lumped components with higher resonance frequency, compatible with Si-based microwave transistors. In this study, novel micromachined lumped passive components on Si substrate have been developed, leading to a drastic improvement in the resonance frequency of inductors. Based on this, an Si/SiGe MMIC technology, combining double mesa-structure Si/SiGe HBT technology and the microma-

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n+ Si	Emitter contact	Sb 2×10^{19} cm^{-3}	2000 Å
n Si	Emitter	Sb 2×10^{18} cm^{-3}	1000 Å
i $Si_{0.6}Ge_{0.4}$			50 Å
p+ $Si_{0.6}Ge_{0.4}$	Base	B 2×10^{19} cm^{-3}	200 Å
i $Si_{0.6}Ge_{0.4}$			50 Å
n- Si	Collector	Sb 5×10^{15} cm^{-3}	3000 Å
n+ Si	Sub-collector	As 1×10^{19} cm^{-3}	15000 Å
p- Si	Substrate	1×10^{12} cm^{-3}	540 μm

Fig. 1. Schematic of the Si/SiGe HBT, in which the As-doped subcollector layer is grown by CVD and the rest of the heterostructure is grown by MBE.

chining technique has been developed. With this technology, X- and Ku-band Si/SiGe monolithic circuits employing micromachined lumped-component matching networks have been successfully implemented for the first time.

In this paper, the details of the Si/SiGe HBT MMIC technology are described in Section II, followed by Section III, describing the performances of active and passive devices. The design and performance of single-, dual-, and three-stage X-band amplifiers and a single-stage Ku-band amplifier are described and discussed in Section IV. Conclusions are made in Section V.

II. Technology

Growth of high-quality epitaxial layers and reproducible and reliable processing are the key factors in the successful development of high-performance devices and circuits. We have grown N-p-N double heterojunction Si/SiGe HBT structures and developed a stable SiGe MMIC process. Two epitaxial techniques are widely used for the growth of Si/SiGe heterostructures: molecular beam epitaxy (MBE) and ultrahigh vaccum/chemical vapor deposition (UHV/CVD). MBE growth benefits from the larger range of doping (10^{14}–10^{21} cm^{-3}) and lower growth temperature, while UHV/CVD growth offers higher throughput, which is favored for mass production [10]. In this study, the HBT heterostructures were grown by MBE, except for the thick subcollector layer (see Fig. 1). The detailed growth sequence is as follows: arsenic-doped subcollector layer (1.5 μm) is grown by CVD on a high-resistivity (100) Si wafer, whose resistivity is higher than 10 k$\Omega\cdot$cm according to a spreading resistance analysis (SRA). Then, the wafer is loaded into the MBE chamber for the growth of the HBT starting with the antimony-doped Si collector layer. The SiGe base layer is doped p-type with boron. Two design issues for the base layer are briefly discussed here: spacer layers and Ge composition profiles. The outdiffusion of boron, which may occur during the epitaxy, processing, and circuit operation, is known to move the p-n junction toward the emitter, away from the Si/SiGe heterojunction. This would give rise to parasitic energy barriers in the conduction band, resulting in the increase of the base transit time τ_B and the reduction of the cutoff frequency f_T [11]. To suppress the boron outdiffusion, intrinsic spacers are frequently introduced as buffer layers. In this study, a 50-Å spacer layer is inserted on both sides of the base layer and no significant outdiffusion effects have been observed. A uniform Ge composition profile of 40% is employed for the SiGe alloy in the base layer. Compared with a graded composition profile (smallest mole fraction at emitter–base (E–B) junction), the uniform profile leads to a larger base transit time τ_B due to the absence of the quasi-electric field. However, the larger band offset at the E–B junction in the case of a uniform profile provides larger current gain β and smaller emitter delay time τ_E [12]. In addition, the larger Ge composition at E–B junction reduces the possibility of overetching the base layer during the selective wet etching of emitter layer in mesa-type HBT processing, since the selectivity is higher for larger Ge composition in SiGe alloy. This leads to a smaller base access resistance. The Ge composition profile is determined by a tradeoff between these parameters, and the uniform profile was favored in this study. Base doping concentration is another issue in device design. SRA results show that the base doping concentration of the structure is 2×10^{19} cm^{-3}, which is believed to be underestimated because the measurement step is of the same order as the base layer thickness. The actual concentration is believed to be close to 1×10^{20} cm^{-3}, including unactivated dopants, which are not considered in SRA. After the growth of the base layer and spacer layers, antimony-doped Si emitter layer and emitter cap layer are successively grown. All the MBE epitaxial layers were grown at a rate of 2 Å/s at a background pressure of 6×10^{-9} torr. The growth temperature was 550 °C for the base layer and 415 °C for the collector and emitter layers.

SiGe MMIC's with double mesa-structure HBT's were fabricated with standard liftoff and etching techniques, using the epitaxial wafers described above. The process starts with emitter metal contact formation (Cr/Au = 500/2000 Å) on the highly doped emitter contact layer by evaporation and liftoff. The metal contact is used as an etch mask for the following base layer-exposure step. The base exposure is the most critical step in the fabrication of mesa-type HBT's since this process directly affects the $f_{\max}$ of the devices through the parasitic base resistance R_B. Hence, this step is discussed here in more detail. Overetching of the base layer and the excessive lateral undercut of emitter sidewall should be avoided to keep the value of R_B small, while moderate undercut and vertical emitter sidewall profile are required for the following self-aligned base metal deposition. To meet these requirements, we have employed an angled emitter contact formation and two-step etching. The latter is performed by the combination of dry and wet etching. First, SF_6 and O_2-based anisotropic reactive ion etch (RIE) removes the biggest portion of the emitter layer without undercut. Second, KOH-based selective solution (KOH:$K_2Cr_2O_7$:H_2O = 50g:2g:200 ml) etches away the remaining emitter layer and stops close to the E–B heterojunction. The etching selectivity of the KOH solution was found to be higher than 10 at 30 °C for Ge composition of 40%. With this two-step etching, the emitter sidewall undercut can be considerably reduced, since the sidewall is laterally etched only during the short wet etching cycle. Fabricated devices show typical undercut of around 1000 Å. The purpose of the angled emitter contact pattern is

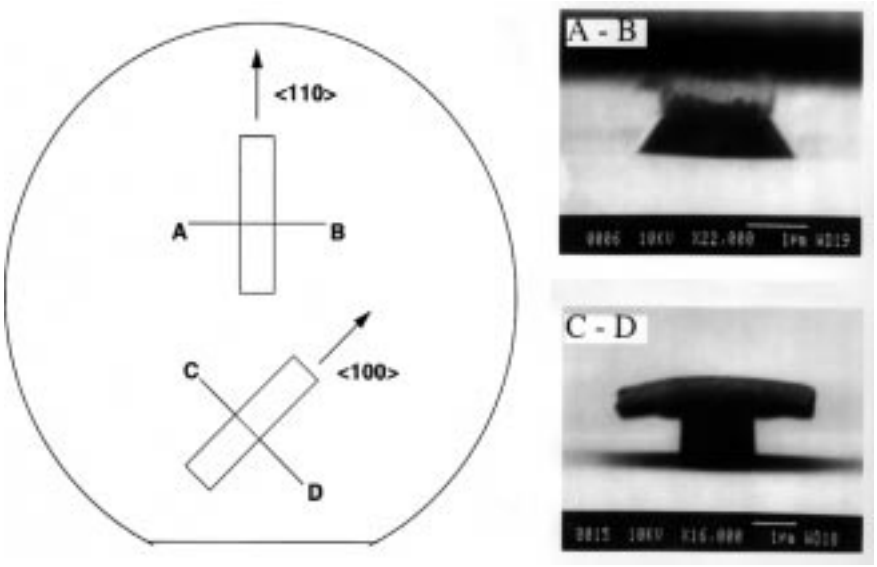


Fig. 2. Orientation dependence of KOH etching profile. A–B: aligned for <110> orientation. C–D: aligned for <100> orientation.

as follows. The etch rate of Si in the KOH-based solution is crystal-orientation dependent, exhibiting much smaller etch rate for <111> orientation compared with those for <100> and <110> orientations [13], [14]. This orientation dependence gives rise to trapezoidal sidewall etch profile when etch mask patterns on <100> wafers are aligned along <110> orientation, which is parallel to the major flat of the wafer. On the other hand, a vertical sidewall profile can be obtained when the etch mask patterns are aligned along <100> orientation, which is 45° off the major flat of <100> wafer. This is depicted in Fig. 2 with scanning electron microscope (SEM) pictures, which show resultant trapezoidal and vertical sidewall profiles for etch mask patterns aligned along <110> orientation (A–B), and <100> orientation (C–D), respectively. Therefore, the self-aligned deposition of base metal, using emitter metal patterns as etch mask for KOH etching, will be successful only if emitter patterns are aligned 45° off the major flat. Otherwise, the base metal will eventually touch the protruding emitter sidewall, electrically shorting the emitter and base. Rapid thermal annealing (RTA) is done for 20 s at 400 °C for the optimized ohmic contact of emitter metal. After the self-aligned base metal deposition (Pt/Au = 200/1300 Å) by evaporation, the base mesa is formed by RIE, exposing the highly doped subcollector layer for collector contact. Collector metal (Ti/Au = 500/2000 Å) contact is defined by evaporation and liftoff, followed by another RTA (3 s, 375 °C) for the base and collector ohmic contact. An RIE step for device isolation completes the processing for active devices, leaving the high-resistivity Si substrate exposed. Passive devices are built on the exposed substrate. Three successive evaporations provide the basic building blocks for metal–insulator–metal (MIM) capacitors; bottom metal layer (Ti/Al/Ti/Au/Ti/Ni = 500/9000/500/3000/500/1500 Å), dielectric layer (SiO = 2000 Å), and top metal layer (Ti/Ni = 500/1000 Å). The bottom metal layer also serves as a feeding line for spiral inductors. A thick intermetal dielectric layer (1 μm SiO_2), which also passivates the HBT's, is next deposited by plasma-enhanced CVD (PECVD). On top of the deposited SiO_2 layer, a thin-film resistor is formed by the evaporation of 500 Å NiCr. Via holes for contacts are opened by selective dry etching of the SiO_2 layer. This is followed by a thick metal (Ti/Al/Ti/Au/Ti/Ni = 500/15 000/500/4000/500/1500 Å) evaporation, which provides device interconnection, probing pads, inductor spirals, and top contact of MIM capacitors. Finally, a two-step deep RIE removes the exposed SiO_2 layer and Si substrate while active devices and resistors are covered with photoresist for protection. This is the micromachining step which improves the resonance frequency of inductors, as will be discussed in more detail in the following section. No airbridge is employed in this process.

III. Device Performance

A. Active Devices: Si/SiGe HBT's

Double mesa-structure Si/SiGe HBT's with various dimensions have been fabricated and their dc and RF properties were measured. The following discussion will focus on the characteristics of devices with emitter area $A_E = 5 \times 5\ \mu m^2$, since these devices have been employed in the design of the amplifiers. The actual emitter area will be $4.8 \times 4.8\ \mu m^2$, if undercut from wet etching is taken into account. The devices have base–collector junction area of $A_{BC} = 12 \times 13\ \mu m^2$, which is also an important parameter for the maximum oscillation frequency f_{max}. The common emitter current–voltage characteristics are shown in Fig. 3(a). As can be seen from the plot, the device suffers from the Kirk effect, which arises from the concentration inversion of injected carriers and space charge in the collector depletion region. This can be ascribed to the relatively low collector doping concentration ($5 \times 10^{15}\ cm^{-3}$) of the device. This effect appears to be more severe for low V_{CE}, since the velocity of the injected carriers is smaller at lower voltage leading to the higher effective carrier concentration. However, the device and circuit operations will not be affected by the Kirk effect, provided the operating

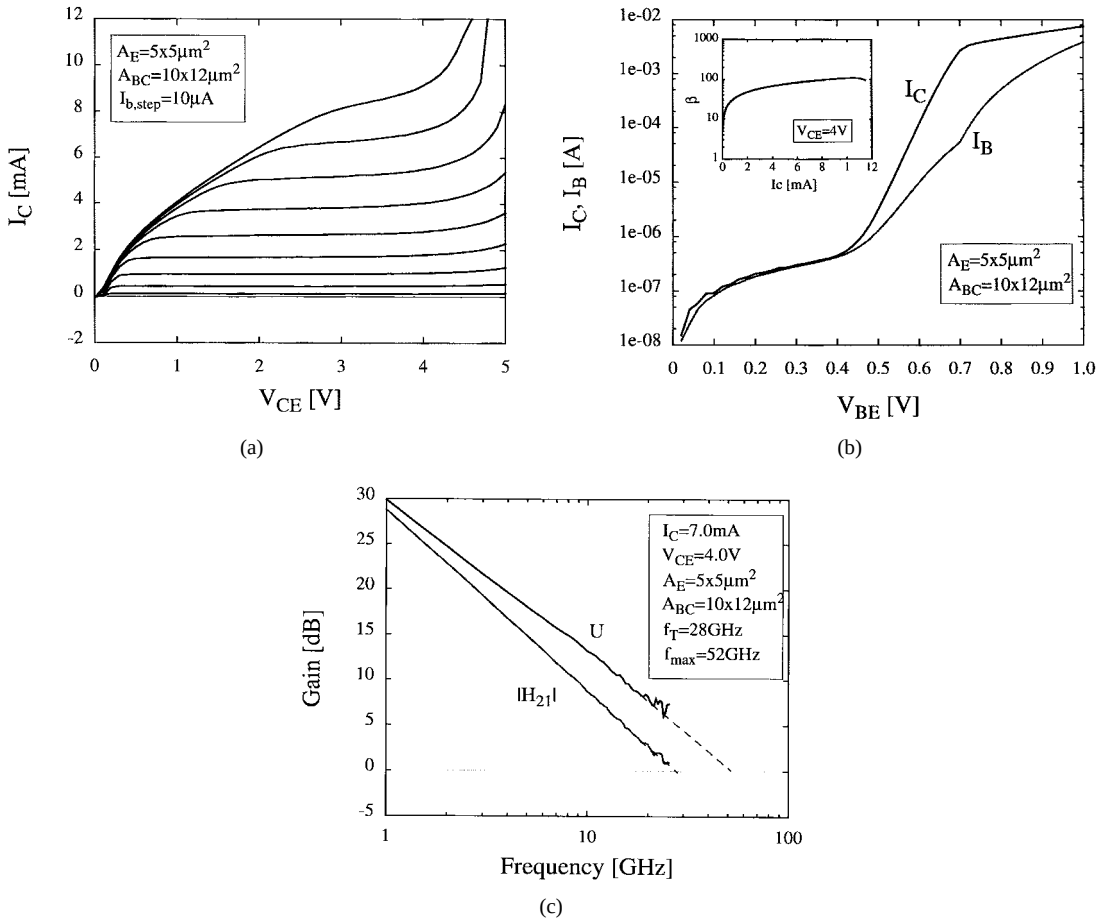
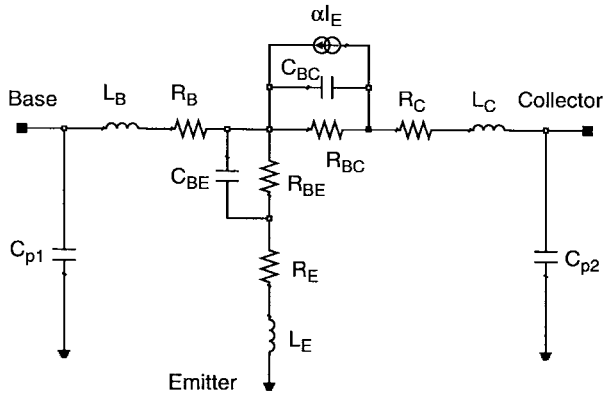


Fig. 3. (a) Measured current–voltage characteristics of an Si/SiGe HBT with emitter area of $5 \times 5\ \mu\text{m}^2$. (b) Gummel plot of the HBT with dc current gain β in the inset. Current gain is measured with $V_{\text{CE}} = 4$ V. (c) Gains $|H_{21}|$ and U of the device measured at $I_C = 7.0$ mA and $V_{\text{CE}} = 4.0$ V. $f_T = 28$ GHz and $f_{\max} = 52$ GHz.

bias point is chosen outside the value for which the Kirk effect is operative and the signal amplitude is not significantly large. The offset voltage of the device is very close to zero, implying the symmetry of E–B and base–collector (B–C) heterojunctions as a consequence of uniform Ge composition across the base layer. Fig. 3(b) shows the Gummel plot of the same device. The collector and base ideality factors are extracted to be $n_c = 1.04$ and $n_b = 1.79$, respectively. The dc current gain β is measured at the fixed collector–emitter voltage $V_{\text{CE}} = 4$ V, as shown in the inset. Values higher than 100 are obtained for most of the operating current range with the maximum value of 109 occurring at $I_C = 10.4$ mA. S-parameters have been measured for a frequency range of 0.5–25.5 GHz with an H8510B network analyzer in order to investigate the RF characteristics of the device. Fig. 3(c) shows the current gain H_{21} and the unilateral power gain U as a function of the frequency at a bias point of $I_C = 7.0$ mA and $V_{\text{CE}} = 4.0$ V. The corresponding f_T and $f_{\max}$, obtained from the extrapolation of $|H_{21}|$ and U on the assumption of -6 dB/octave rolloff, are 28 and 52 GHz, respectively. Higher $f_{\max}$ values could be obtained if the lateral dimension of the device is optimized for smaller base spreading resistance. The measured S-parameters have been utilized for the small-signal modeling of the device with an HBT T-model. The equivalent circuit is given in Fig. 4, along with the corresponding parameters extracted from the method proposed in [15].

B. Micromachined Passive Components

Planar lumped inductors are widely used in MMIC's as matching elements, bias chokes, and filter components. Compared with distributed transmission-line components, lumped components are smaller, especially at frequencies below 30 GHz. As a result, lumped component circuits can be more compact than the distributed ones in MMIC applications. However, planar lumped components suffer from parasitic effects. In particular, planar lumped spiral inductors exhibit very low resonance frequencies due to the parasitic capacitance, thus limiting operating frequencies. Work has been done by fabricating the inductors on a dielectric membrane to increase the resonance frequency [16], [17]. This technique is difficult to adopt for integration with active devices since it requires the development of a dielectric membrane between the bulk high-resistivity Si and the doped layers. Recently, an air–gap stacked spiral inductors using air–bridge technology has been introduced [18]. By stacking metal lines, inductor area can be reduced by 25%–45% and the resonance frequencies can be increased by 10%–15%



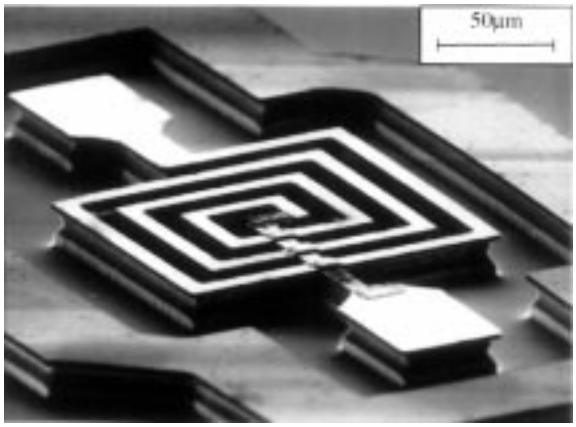
R_B	13.1 Ω
L_B	62.6 pH
R_{BE}	1.0 Ω
C_{BE}	106.8 fF
R_E	15.8 Ω
L_E	141.7 pH
R_{BC}	127.0 kΩ
C_{BC}	28.9 fF
R_C	24.8 Ω
L_C	66.1 pH
$C_{p1,2}$	4.0 fF
α_o	0.995

Fig. 4. T-model small-signal equivalent circuit of HBT and circuit elements extracted from S-parameter measurements.

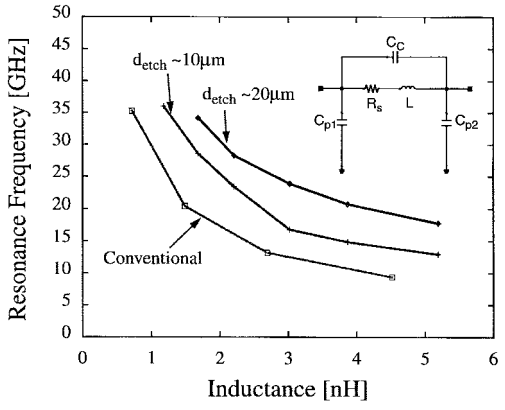
compared with conventional spiral inductors. However, the increase in resonance frequencies is not enough for MMIC applications in Ku-band or higher.

To obtain an inductor with higher resonance frequency, a new micromachined spiral inductor has been developed, as shown in Fig. 5(a). In this inductor structure, a bottom metal layer and interconnection metal layer, separated by an intermetal PECVD SiO_2 layer, form the feed line and spirals of inductors, respectively. By covering the metal structure with Ni, which is used as a self-aligned mask, and removing the exposed PECVD SiO_2 layer and Si substrate material in between the turns by RIE, the effective dielectric constant of this structure can be reduced. This results in a smaller series and shunt parasitic capacitance from turn to turn (C_C) and from the signal line to ground (C_P), as shown in the equivalent circuit of the inductor [inset to Fig. 5(b)]. Due to the significant reduction of the parasitics, the resonance frequency can be increased drastically. The resonance frequencies are extracted from two-port S-parameter measurement of the inductors up to 40 GHz with an HP8510C network analyzer. Fig. 5(b) shows the resonance frequencies of the micromachined inductors and conventional ones. Compared with conventional spiral inductors, a 50% improvement in resonance frequencies can be obtained by a 10-μm-deep RIE, and the improvement can be as high as 100% if a 20 μm-deep RIE is used.

MIM capacitors have also been fabricated and characterized. As mentioned earlier, evaporated SiO film ($d = 2000$ Å) is used as a dielectric material and sandwiched by bottom and top metal layers. Top metal layer protects the dielectric film during via hole opening process and the top feeding contact is provided by much thicker interconnection metal to reduce the parasitic resistance and inductance. SiO is preferred to SiO_2 as a dielectric film, since SiO provides higher dielectric constant, leading to smaller capacitor area. The dielectric constant ϵ_r of the evaporated SiO, extracted from the capacitance and the area of fabricated capacitors, is 4.7, which provides a capacitance of 0.21 fF/μm^2. The measured capacitors exhibit resonance frequencies higher than 20 GHz up to 1 pF. Since the capacitance values of the matching capacitors in X- and Ku-band applications rarely exceed 1 pF, these capacitors can safely be applied to circuits at these bands.



(a)



(b)

Fig. 5. (a) Photomicrograph of a micromachined spiral inductor with etch depth of 20 mm. (b) Measured resonance frequencies of inductors with various etch depth d_{etch} with equivalent circuit of spiral inductor (inset). C_{P1} and C_{P2} represent parasitic capacitance between inductor and ground. C_C is parasitic coupling capacitance. R_S is parasitic series resistance. L is the inductance.

Thin-film resistors are indispensable components in most microwave circuits, frequently applied to bias circuits and feedback loops. 500-Å NiCr film was evaporated to realize thin-film resistors. The sheet resistance of the film is found to be in the range of 45–50 $\Omega/\square$.

Interconnection line sections were fabricated and characterized since they are frequently employed to connect adjacent components on circuits. They can be considered as electrical shorts in low-frequency operations, but they behave mainly as inductors in the microwave frequency range, and their effect have to be considered for rigorous microwave-circuit designs. The inductance of line sections shows fairly linear relation with the length of the line, which implies that the total inductance is dominated by self-inductance rather than mutual inductance. The inductance per unit length of 2.2-μm-thick 10-μm-wide line sections is found to be around 1.1 pH/μm. Interconnection line sections may be inserted to circuits on purpose for a fine tuning of inductance matching of circuits.

The test structures for all these passive components were fabricated with various dimensions, which cover the entire range of practical interest. S-parameters were measured for the fabricated test patterns and used for modeling with appropriate equivalent circuits including parasitic elements. This completes the passive components library to be used for subsequent circuit design.

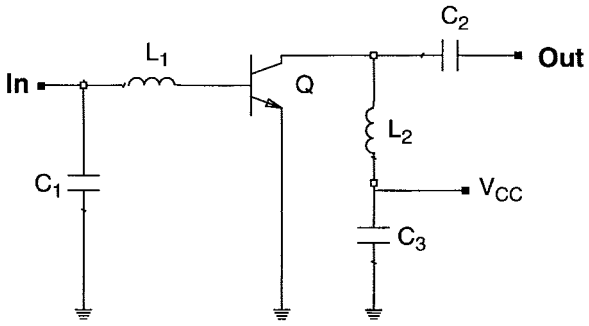
IV. Amplifier Design and Performance

After fabrication and characterization of active devices and passive components, the measured S-parameters and equivalent-circuit parameters are utilized for circuit design. In this study, X-band single-, dual-, and three-stage Si/SiGe HBT amplifiers have been designed, fabricated, and characterized. Preliminary results of a Ku-band single-stage amplifier are also described and discussed.

A. Single-Stage Amplifier

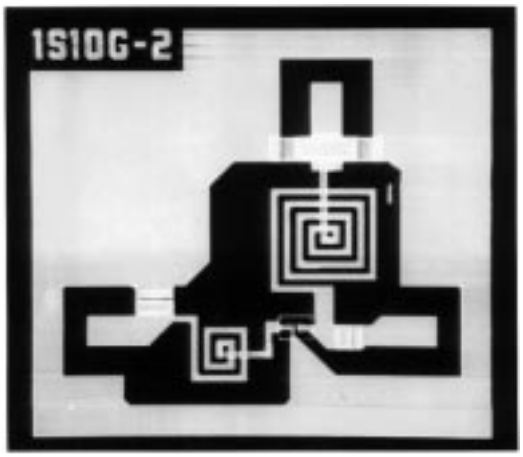
Fig. 6(a) shows the circuit diagram of the X-band single-stage amplifier. Basically, it consists of one Si/SiGe HBT common emitter amplifying stage, along with input and output matching networks and bias circuit. L_1 and C_1 provide conjugate power matching to the input of amplifying stage, while L_2 and C_2 are employed for output power matching. L_2 also functions as an RF choke. This, together with the bypass capacitor C_3, isolates V_{CC} from the amplifier. Base current is supplied from the input of the circuit, together with input RF signal.

The photomicrograph of the fabricated circuit is shown in Fig. 6(b). The chip size is 0.75 × 0.65 mm^2. Considering that circuits with distributed matching components usually stretch up to around a half-wavelength at the operating frequency, this chip size may be less than 20% of the corresponding distributed matching circuit. The S-parameters of the fabricated circuit was measured with an HP8510C network analyzer with dc-bias supplies from an HP4145B semiconductor parameter analyzer. The measured transducer power gain S_{21} is shown in Fig. 6(c), along with input and output return losses S_{11} and S_{22} at the bias of $V_{\rm CE} = 4.7$ V and $I_C = 9.9$ mA. The bias was optimized for maximum gain. A peak gain of 4.0 dB occurs at 10.0 GHz. The output return loss S_{22} has a minimum value less than −20 dB, which is reasonably low. However, the minimum value of input return loss S_{11} is only around −7 dB. This may be explained by the process variations which would change parasitic values of devices, thus leading to shifts in S-parameters. Input and output voltage standing wave ratios

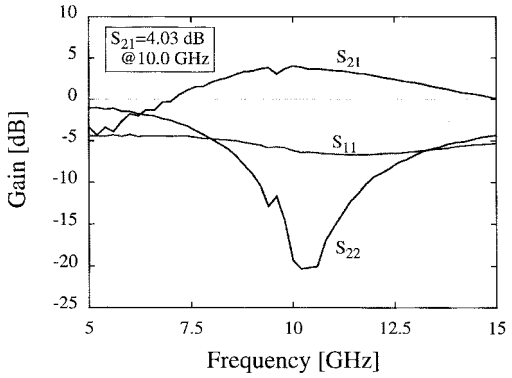


C_1	0.20 pF	L_1	0.51 nH
C_2	0.13 pF	L_2	1.80 nH
C_3	0.78 pF	-	-

(a)



(b)



(c)

Fig. 6. X-band single-stage amplifier. (a) Circuit diagram. (b) Photomicrograph of fabricated circuit. The chip size is 0.75 × 0.65 mm^2. (c) Measured transducer power gain S_{21}, input return loss S_{11}, and output return loss S_{22}.

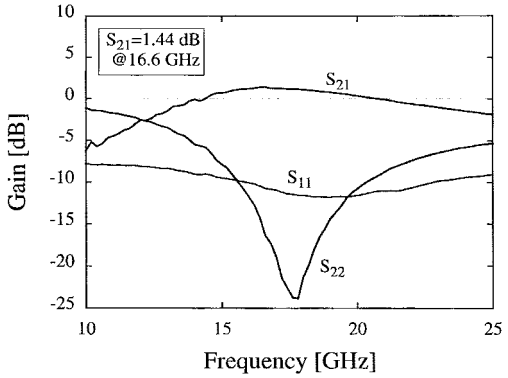


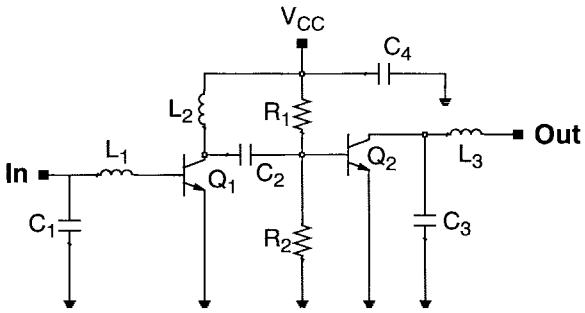
Fig. 7. Measured transducer gain S_{21}, input return loss S_{11}, and output return loss S_{22} of Ku-band single-stage amplifier.

(VSWR's), calculated from the input and output return losses, exhibit minimum values of 2.73 and 1.21, respectively.

A Ku-band single-stage amplifier was also designed and fabricated. The circuit configuration is basically same as X-band version. Only the passive component values are changed to meet the new matching condition at Ku-band. The complete circuit occupies an area of 0.62 $\times$ 0.64 mm^2, which is slightly smaller than the X-band circuit due to smaller passive-element dimensions required for higher frequency. The horizontal dimension of the circuit is still less than one-eighth of the wavelength, suggesting that the advantage of lumped matching is still obvious for Ku-band in terms of circuit area. The gain and return losses are shown in Fig. 7. The gain S_{21} exhibits a peak value of 1.4 dB at a frequency of 16.6 GHz and the gain keeps positive values over 20 GHz, reaching K-band. The input return loss S_{22} is close to -25 dB and the output return loss S_{11} exceeds -11 dB. The input and output VSWR of the amplifier have the minimum values of 1.69 and 1.14, respectively.

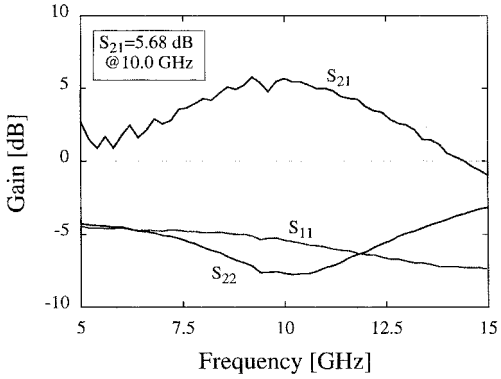
B. Dual-Stage Amplifier

A dual-stage amplifier is designed with a similar approach as the single-stage amplifier and its schematic is shown in Fig. 8. It consists of two common emitter stages and three matching networks. Input matching is provided by elements L_1 and C_1 as in the single-stage amplifier. L_2 and C_2, and L_3 and C_3 constitute interstage and output matching networks, respectively. C_2 also functions as a blocking capacitor separating the first and second amplifying stages dc-wise, and L_2 behaves as an RF choke, as in the case of the single-stage amplifier. V_{CC} supplies collector voltage for the first stage and, simultaneously, base current for the second stage via a resistor voltage divider. R_1 and R_2 values were carefully selected to give a accurate base–emitter voltage for optimum bias since the base current is very sensitive to the voltage across base and emitter. The resistor values are liable to change from process to process since the film is too thin (500 Å) to be accurately controlled by evaporation. However, the ratio of R_1 and R_2 is unchanged, even if the absolute resistance values fluctuate, leading to a stable base current supply at the input of the second stage. The base current for the first stage and the collector voltage for the second stage are supplied through the input and output port of the amplifier, respectively. The chip size is 0.98 $\times$ 0.80 mm^2, which is 60% larger than that for the single-stage amplifier. In this context, it is apparent that the area per stage reduces as the number of stages increases. The gain is 5.7 dB at 10.0 GHz and the input and output return loss remains between -5 and -10 dB [see Fig. 8(b)]. The higher complexity of the circuit, compared with single-stage amplifier, is believed to result in poor return loss and lower gain per stage.



C_1	0.11 pF	C_4	0.78 pF	L_3	1.20 nH
C_2	0.18 pF	L_1	0.37 nH	R_1	1400 Ω
C_3	0.10 pF	L_2	1.55 nH	R_2	400 Ω

(a)

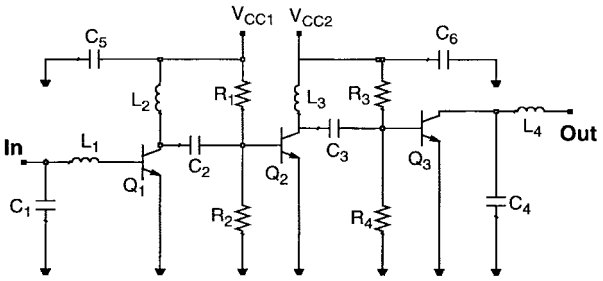


(b)

Fig. 8. X-band dual-stage amplifier. (a) Circuit diagram. (b) Measured transducer gain S_{21}, input return loss S_{11}, and output return loss S_{22}.

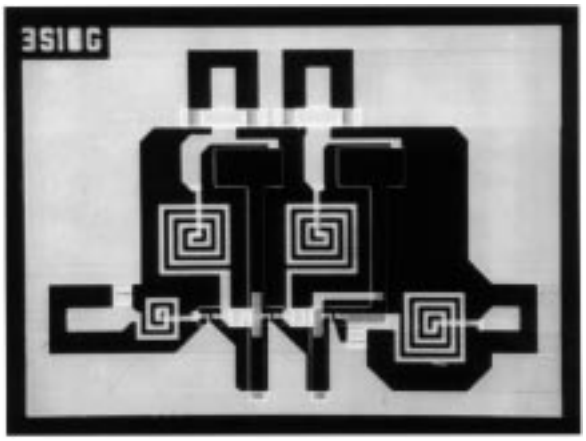
C. Three-Stage Amplifier

A three-stage amplifier is designed in a manner similar to the single- and dual-stage amplifiers. Three common emitter amplifying stages and four matching networks are the basic building blocks for the amplifier [see Fig. 9(a)]. Similar to the dual-stage amplifier case, V_{CC1} supplies collector voltage to the first stage and base current for the second stage, while V_{CC2} supplies collector voltage and base current for the second and third stage, respectively. L_2 and L_3 are employed for both matching elements and RF chokes, while C_2 and C_3 serve as matching components as well as blocking capacitors. Base current for the first stage and collector voltage for the third stage are supplied from the input and output port, respectively. The chip size is 1.15 $\times$ 0.84 mm^2, as shown in Fig. 9(b).

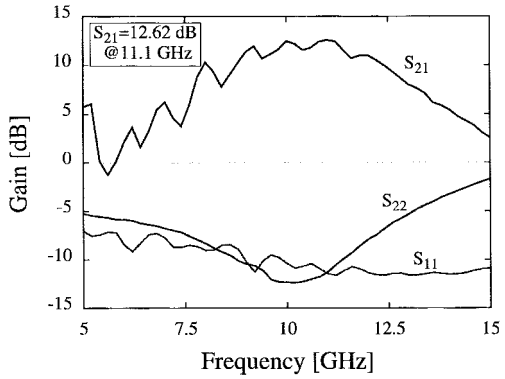


C_1	0.10 pF	C_6	0.78 pF	R_1	1400 Ω
C_2	0.18 pF	L_1	0.38 nH	R_2	400 Ω
C_3	0.17 pF	L_2	1.46 nH	R_3	1400 Ω
C_4	0.10 pF	L_3	1.55 nH	R_4	400 Ω
C_5	0.78 pF	L_4	1.20 nH	-	-

(a)



(b)



(c)

Fig. 9. X-band three-stage amplifier. (a) Circuit diagram. (b) Photomicrograph of fabricated circuit. The chip size is 1.15 × 0.84 mm^2. (c) Measured transducer gain S_{21}, input return loss S_{11}, and output return loss S_{22}.

The area per stage is 0.32 mm^2, 60% of the single-stage amplifier. The measured data are shown in Fig. 9(c). The peak gain is 12.6 dB, occurring at 11.1 GHz. The input and output return losses are found to be between −10 and −15 dB. Ripples can be seen in the plots. These may be attributed to either extrinsic or intrinsic factors. Extrinsic factors usually involve the measurement environment connected to the device-under-test (DUT). Occasionally, the bias supply affects the operation of the circuits-under-test if the isolation of the bias probes is poor. RF choke and bypass capacitors have been employed to isolate the amplifiers under study from the bias probes. This technique may provide insufficient isolation, leading to fluctuations arising from the loading effect. Intrinsic factors are closely related to the stability of the amplifier, which was taken into account in the design to avoid the unstable region in the determination of matching points for each stage. However, process variations may have changed the S-parameters of active devices, resulting in the shift of stability circles on the Γ plane. Extracted stability factor K and $|\Delta|$ ($\Delta = S_{11}S_{22} - S_{21}S_{12}$) of the amplifier indicate the unconditional stability of the complete circuit in the whole frequency band, but this does not fully guarantee the stability of individual stages. Further investigation is necessary to locate the exact source of the fluctuations.

V. Conclusion

X- and Ku-band amplifiers, based on Si/SiGe HBT's, and a novel micromachined passive component technology have been designed, fabricated, and characterized. The fabricated double mesa-structure Si/SiGe HBT ($A_E = 5 \times 5$ μm^2) exhibited a dc current gain of 109, and f_T and $f_{\max}$ of 28 and 52 GHz, respectively. Micromachined spiral inductors demonstrated improved resonance frequency by a factor of more than two, compared with devices made with conventional processing. This broadens the applicable frequency range of lumped component circuits, leading to reduced chip size at high frequencies. Characteristics of capacitors, resistors, and line sections have also been investigated. Modeling of fabricated active and passive components was carried out with appropriate equivalent circuits and applied to the design of X- and Ku-band amplifiers. X-band single-stage amplifiers exhibit a peak gain of 4.0 dB at 10.0 GHz, while dual- and three-stage amplifiers exhibit peak gains of 5.7 dB at 10.0 GHz and 12.6 dB at 11.1 GHz, respectively. Ku-band single-stage amplifier showed a peak gain of 1.4 dB at 16.6 GHz. Minimum circuit area per stage was obtained from three-stage amplifier as 0.32 mm^2 in X-band.

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